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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,964	05/19/2004	Shriram Ramanathan	42P19016	8073

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EXAMINER	
DINH, BACH T	

ART UNIT	PAPER NUMBER
1795	

MAIL DATE	DELIVERY MODE
10/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,964	RAMANATHAN ET AL.	
	Examiner	Art Unit	
	BACH T. DINH	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8-11 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8-11 and 21-25* is/are rejected.

7)☒ Claim(s) *6 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/14/2009 has been entered.

Summary

2. This is the response to the communication filed on 08/14/2009.

3. Claims 6, 8-11 and 21-25 remain pending in the application.

4. All of previous rejections are withdrawn in view of applicant's amendment to the claims.

5. The application is not in condition for allowance.

Claim Objections

6. Claim 6 is objected to because of the following informalities: the word "absense" in line 13 is believed to be the misspelled of absence. Appropriate correction is required.

7. Claim 21 is objected to because of the following informalities: the word "absense" in line 14 is believed to be the misspelled of absence. Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. (US 7,038,312) in view of Chu et al. (US 6,804,966) and Rabin et al. (WO 03/046265).

Addressing claim 6 and 8-10, Khan discloses an electronic package, comprising:

A microelectronic die (102, figure 1B) having at least one area of which is of a higher heat dissipation rate than the remainder of the microelectronic die when in operation (figure 2B, area 202 is the die mounting position with the center area being the area with the highest temperature or the area with a higher heat dissipation rate than the remainder of the microelectronic die);

Furthermore, Khan discloses stiffener 112 is coupled to the electronic die 102 for heat spreading purpose (6:16-17, figure 1B) and the stiffener 112 is made of copper, tin or aluminum (6:13-15). Moreover, the temperature profile in figure 2B shows that the

center area has the highest temperature, which is concentrically surrounded by areas with successively lower temperatures. Overall, figure 2B shows at least 4 areas with different temperatures that concentrically surrounding each other, with the center area being the claimed area of higher heat dissipation rate and the area adjacent to the center area with lower temperature is claimed intermediate area. Both of the higher heat dissipation area and the intermediate area are concentrically surrounded by areas of even lower temperatures.

Khan is silent regarding a first electrode proximate to the microelectronic die, a dielectric material proximate to the first electrode, a second electrode opposing the first electrode with the dielectric material disposed therebetween, a plurality of nano-wires extending between the first and second electrode with the density of the nano-wires being arranged in the configuration as required by current claim.

Rabin discloses a thermoelectric cooling device (figures 8-9); wherein, the thermoelectric cooling device comprises of:

A first electrode proximate the higher heat area (high temperature electrode 260);

A dielectric material proximate the first electrode (porous alumina body 220, 13:26-31);

A second electrode opposing the first electrode with the dielectric material disposed therebetween (electrodes 230); and

A plurality of nano-wires extending between the first electrode and the second electrode (p-type and n-type bismuth containing nanowires 222 and 224, 9:25-31, 13:32-14:2).

Chu discloses a thermoelectric package (figures 1-3B), comprising:

A microelectronic die (electronic device 12) having at least one area of which is of a higher heat dissipation rate than the remainder of the microelectronic die when in operation (figures 2A-2C, high heat flux area 13 and the remaining lower heat flux area of device 12);

A plurality of thermoelectric elements disposed at highest density in the high heat flux area 100A and 100B and lower density at the low heat flux area 110 (figures 3A-3B, 6:40-67).

At the time of the invention, one with ordinary skill in the art would have found it obvious to modify the electronic package of Khan with coupling the thermoelectric package of Rabin to the electronic die 102 of Khan in the manner disclosed by Chu because Chu discloses that it is conventional in the art to use a thermoelectric package for controlling the temperature of an electronic die and the thermoelectric package of Rabin is capable of spreading heat from one area to another (Rabin, 12:20-13:7) as well as converting heat to electrical energy, thus functioning as an additional power generator (Rabin, 13:18-25). According to the disclosure of Chu, where the density of the thermoelectric elements is arranged according to the temperature profile of the electronic die, one would have found it obvious to arrange the nano-wires of Rabin with the highest density proximate to the center area of Khan's electronic die with the highest temperature, follow by surrounding the center area with a lower density of nano-wires proximate to the intermediate area, a further lower density of the nano-wires proximate to the area surrounding the intermediate area and an absence of nano-wires proximate to the

remainder of the microelectronic die because doing so would provide more uniform temperature distribution across the electronic device as well as improving the energy consumption efficiency of the thermoelectric package (Chu, 7:1-13).

Khan, Rabin and Chu are silent regarding the nano-wires being arranged in concentric ovals as required by current claim. However, it does not appear that the concentric ovals arrangement is critical to the instant application for such concentric ovals arrangement is designed to match the temperature profile of the electronic die (figure 13 of current application); furthermore, Chu already discloses the method of arranging the density of the nano-wires to match the temperature profile of an electronic die as addressed above. Therefore, the arrangements of the nano-wires are selectable variables of which the selection of shape would be within the technical grasp of an ordinary artesian based on the size, shape and the location of the intended installation/application. Thus, absent contrary support for the criticality of the claimed concentric ovals arrangement, it would have been a matter of obviousness to a person having ordinary skill in the art at the time of the invention to vary/select the shape of the arrangement of the nano-wires in the thermoelectric package of Khan, Chu and Rabin (see MPEP 2144.04{IV}{B}).

Addressing claim 11, Rabin discloses a negatively charged trace electrically connected to the first electrode (for cooling function as described in figure 8A, the negatively charged p-type nanowires 222 are connected to the electrode 260) and a positively charged trace to the second electrode (in figure 8A, the n-type nanowires 224 are positively charged, 12:29-13:7).

11. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. (US 2002/0145194) in view of Khan et al. (US 7,03,312), Rabin et al. (WO 03/046265) and Chu et al. (US 6,804,966).

Addressing claims 21-24, Addressing claims 21-24, O'Connor discloses an electronic system (figure 1), comprising:

An external substrate within a housing (circuit board of the electronic assembly within a housing for computers, wireless communication devices or entertainment devices, 1:12-27); and

At least one microelectronic device package (integrated circuit package disclosed in figures 3a-3c) attached the external substrate (integrated circuit is physically and electrically coupled to the circuit board, 1:12-27). In figures 3a-3c, O'Connor discloses the integrated circuit package includes a die 40 comprises of a heat spreading layer 100, which can be made of nanotubes (6:45-47), and the heat spreading layer must be thermally connected to the areas of the die that will generate the most heat [0042];

An input device interfaced with the external substrate (figure 1, keyboard/controller 20);

A display device interfaced with the external substrate (figure 1, display 8);

All the components are interfaced via a system bus 2; and

In figure 7a, O'Connor also discloses the microelectronic die 40 has area of highest heat dissipation rate (100-110 °C), areas of intermediate heat dissipation rate (90-100°C) surrounding the area of highest heat dissipation rate, an area of lower heat dissipation rate

(80-90 °C) surrounding the area of intermediate heat dissipation rate, and an area of even lower heat dissipation rates or the remainder of the microelectronic die surrounding the area of lower heat dissipation rate (80-90 °C).

O'Connor is silent regarding a first electrode proximate to the microelectronic die, a dielectric material proximate to the first electrode, a second electrode opposing the first electrode with the dielectric material disposed therebetween, a plurality of nano-wires extending between the first and second electrode with the density of the nano-wires being arranged in the configuration as required by current claim.

Khan discloses a microelectronic die (102, figure 1B) having at least one area of which is of a higher heat dissipation rate than the remainder of the microelectronic die when in operation (figure 2B, area 202 is the die mounting position with the center area being the area with the highest temperature or the area with a higher heat dissipation rate than the remainder of the microelectronic die). Moreover, the temperature profile in figure 2B shows that the center area has the highest temperature, which is concentrically surrounded by areas with successively lower temperatures. Overall, figure 2B shows at least 4 areas with different temperatures that concentrically surrounding each other, with the center area being the claimed area of higher heat dissipation rate and the area adjacent to the center area with lower temperature is claimed intermediate area. Both area of higher heat dissipation and the intermediate area are concentrically surrounded by areas of even lower temperatures.

Rabin discloses a thermoelectric cooling device (figures 8-9); wherein, the thermoelectric cooling device comprises of:

A first electrode proximate the higher heat area (high temperature electrode 260);

A dielectric material proximate the first electrode (porous alumina body 220, 13:26-31);

A second electrode opposing the first electrode with the dielectric material disposed therebetween (electrodes 230); and

A plurality of nano-wires extending between the first electrode and the second electrode (p-type and n-type bismuth containing nanowires 222 and 224, 9:25-31, 13:32-14:2).

Chu discloses a thermoelectric assembly; wherein, the density of the thermoelectric elements is adjusted according to the degree of heat flux at different area of an integrated circuit chip 12 (figures 3A-3B, 6:40-67, denser thermoelectric elements in higher heat flux areas 100A and 100B and less dense thermoelectric elements at area of lower heat flux 110).

At the time of the invention, one with ordinary skill in the art would have found it obvious to modify the electronic package of O'Connor with the microelectronic die of Khan because the microelectronic die of Khan has improved heat spreading capabilities as well as providing high levels of IC electrical performance (Khan, 2:22-24). Furthermore, one with ordinary skill in the art would have found it obvious to modify the microelectronic die of Khan with coupling the thermoelectric package of Rabin to the microelectronic die 102 in the manner disclosed by Chu because Chu discloses that it is conventional in the art to use a thermoelectric package for controlling the temperature of an electronic die and the thermoelectric package of Rabin is capable of spreading heat

from one area to another (Rabin, 12:20-13:7) as well as converting heat to electrical energy, thus functioning as an additional power generator (Rabin, 13:18-25). According to the disclosure of Chu, where the density of the thermoelectric elements is arranged according to the temperature profile of the electronic die, one would have found it obvious to arrange the nano-wires of Rabin with the highest density proximate to the center area of Khan's electronic die with the highest temperature, followed by surrounding the center area with a lower density of nano-wires proximate to the intermediate area, a further lower density of the nano-wires proximate to the area surrounding the intermediate area and an absence of nano-wires proximate to the remainder of the microelectronic die because doing so would provide more uniform temperature distribution across the electronic device as well as improving the energy consumption efficiency of the thermoelectric package (Chu, 7:1-13).

O'Connor, Khan, Rabin and Chu are silent regarding the nano-wires being arranged in concentric ovals as required by current claim. However, it does not appear that the concentric ovals arrangement is critical to the instant application for such concentric ovals arrangement is designed to match the temperature profile of the electronic die (figure 13 of current application); furthermore, Chu already discloses the method of arranging the density of the nano-wires to match the temperature profile of an electronic die as addressed above. Therefore, the arrangements of the nano-wires are selectable variables of which the selection of shape would be within the technical grasp of an ordinary artesian based on the size, shape and the location of the intended installation/application. Thus, absent contrary support for the criticality of the claimed

concentric ovals arrangement, it would have been a matter of obviousness to a person having ordinary skill in the art at the time of the invention to vary/select the shape of the arrangement of the nano-wires in the thermoelectric package of Khan, Chu and Rabin (see MPEP 2144.04{IV}{B}).

Addressing claim 25, Rabin discloses a negatively charged trace electrically connected to the first electrode (for cooling function as described in figure 8A, the negatively charged p-type nanowires 222 are connected to the electrode 260) and a positively charged trace to the second electrode (in figure 8A, the n-type nanowires 224 are positively charged, 12:29-13:7).

12. Claims 6, 8-11 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. (US 2002/0145194) in view of Rabin et al. (WO 03/046265) and Chu et al. (US 6,804,966).

Addressing claim 6 and 8-10, O'Connor discloses a thermoelectric package (figures 3a-3c), comprising:

A microelectronic die (die 40) having at least one area of which is of a higher heat dissipation rate than the remainder of the microelectronic die when in operation (figures 7a-7b); in figure 7a, O'Connor also discloses the microelectronic die 40 has area of highest heat dissipation rate (100-110 ^{o}C), which is surrounded by an area of intermediate heat dissipation rate (90-100^{o}C), which is further surrounded by an area of lower heat

dissipation rate (80-90°C), which is also surrounded by the remainder of the microelectronic die having lower temperature.

O'Connor further discloses the heat spreading layer of microelectronic die 40 is made up of nanotubes [0048] and the heat spreading layer must be thermally connected to the areas of the die that will generate the most heat [0042].

O'Connor is silent regarding a first electrode proximate to the microelectronic die, a dielectric material proximate to the first electrode, a second electrode opposing the first electrode with the dielectric material disposed therebetween, a plurality of nano-wires extending between the first and second electrode with the density of the nano-wires being arranged in the configuration as required by current claim.

Rabin discloses a thermoelectric cooling device (figures 8-9); wherein, the thermoelectric cooling device comprises of:

A first electrode proximate the higher heat area (high temperature electrode 260);

A dielectric material proximate the first electrode (porous alumina body 220, 13:26-31);

A second electrode opposing the first electrode with the dielectric material disposed therebetween (electrodes 230); and

A plurality of nano-wires extending between the first electrode and the second electrode (p-type and n-type bismuth containing nanowires 222 and 224, 9:25-31, 13:32-14:2).

Chu discloses a thermoelectric assembly; wherein, the density of the thermoelectric elements is adjusted according to the degree of heat flux at different area of an integrated

circuit chip 12 (figures 3A-3B, 6:40-67, denser thermoelectric elements in higher heat flux areas 100A and 100B and less dense thermoelectric elements at area of lower heat flux 110).

At the time of the invention, one with ordinary skill in the art would have found it obvious to modify the device of O'Connor with the thermoelectric cooling device of Rabin because the cooling device of Rabin is capable of dissipating heat from one area to another (Rabin, 12:20-13:7) as well as converting heat to electrical energy, thus functioning as an additional power generator (Rabin, 13:18-25).

Furthermore, one would have found it obvious to modify the device of O'Connor by adjusting density of the thermoelectric elements according to the temperature profile of the microelectronic die 40 of O'Connor in the manner disclosed by Chu because doing so would allow for lower circuit temperature for a given heat load to be established, provide a more uniform temperature distribution across the electronic device and improve the efficiency of the thermoelectric assembly (Chu, 7:5-13). Specifically, arranging the nano-wires with the higher density proximate to the area of higher temperature (100-110°C), surrounding the area of higher temperature with a lower density of nano-wires proximate to area of intermediate temperature (90-100°C) between the area of higher temperature (100-110 °C) and the remainder of the microelectronic die, surrounding the lower density area with a further lower density proximate to an area of lower temperature (80-90 °C), and an absence of nano-wires at the area of lowest temperature (50-60 °C), which is proximate to the remainder of the microelectronic die.

O'Connor, Rabin and Chu are silent regarding the nano-wires being arranged in concentric ovals as required by current claim. However, it does not appear that the concentric ovals arrangement is critical to the instant application for such concentric ovals arrangement is designed to match the temperature profile of the electronic die (figure 13 of current application); furthermore, Chu already discloses the method of arranging the density of the nano-wires to match the temperature profile of an electronic die as addressed above. Therefore, the arrangements of the nano-wires are selectable variables of which the selection of shape would be within the technical grasp of an ordinary artesian based on the size, shape and the location of the intended installation/application. Thus, absent contrary support for the criticality of the claimed concentric ovals arrangement, it would have been a matter of obviousness to a person having ordinary skill in the art at the time of the invention to vary/select the shape of the arrangement of the nano-wires in the thermoelectric package of O'Connor, Chu and Rabin (see MPEP 2144.04{IV}{B}).

Addressing claim 11, Rabin discloses a negatively charged trace electrically connected to the first electrode (for cooling function as described in figure 8A, the negatively charged p-type nanowires 222 are connected to the electrode 260) and a positively charged trace to the second electrode (in figure 8A, the n-type nanowires 224 are positively charged, 12:29-13:7).

Addressing claims 21-24, O'Connor discloses an electronic system (figure 1), comprising:

An external substrate within a housing (circuit board of the electronic assembly within a housing for computers, wireless communication devices or entertainment devices, 1:12-27); and

At least one microelectronic device package (integrated circuit package disclosed in figures 3a-3c) attached the external substrate (integrated circuit is physically and electrically coupled to the circuit board, 1:12-27). In figures 3a-3c, O'Connor discloses the integrated circuit package includes a die 40 comprises of a heat spreading layer 100, which can be made of nanotubes (6:45-47), and the heat spreading layer must be thermally connected to the areas of the die that will generate the most heat [0042];

An input device interfaced with the external substrate (figure 1, keyboard/controller 20);

A display device interfaced with the external substrate (figure 1, display 8);

All the components are interfaced via a system bus 2; and

In figure 7a, O'Connor also discloses the microelectronic die 40 has area of highest heat dissipation rate (100-110 ^{o}C), areas of intermediate heat dissipation rate (90-100^{o}C) surrounding the area of highest heat dissipation rate, an area of lower heat dissipation rate (80-90 ^{o}C) surrounding the area of intermediate heat dissipation rate, and an area of even lower heat dissipation rates or the remainder of the microelectronic die surrounding the area of lower heat dissipation rate (80-90 ^{o}C).

O'Connor is silent regarding a first electrode proximate to the microelectronic die, a dielectric material proximate to the first electrode, a second electrode opposing the first electrode with the dielectric material disposed therebetween, a plurality of nano-wires extending between the first and second electrode with the density of the nano-wires being arranged in the configuration as required by current claim.

Rabin discloses a thermoelectric cooling device (figures 8-9); wherein, the thermoelectric cooling device comprises of:

A first electrode proximate the higher heat area (high temperature electrode 260);

A dielectric material proximate the first electrode (porous alumina body 220, 13:26-31);

A second electrode opposing the first electrode with the dielectric material disposed therebetween (electrodes 230); and

A plurality of nano-wires extending between the first electrode and the second electrode (p-type and n-type bismuth containing nanowires 222 and 224, 9:25-31, 13:32-14:2).

Chu discloses a thermoelectric assembly; wherein, the density of the thermoelectric elements is adjusted according to the degree of heat flux at different area of an integrated circuit chip 12 (figures 3A-3B, 6:40-67, denser thermoelectric elements in higher heat flux areas 100A and 100B and less dense thermoelectric elements at area of lower heat flux 110).

At the time of the invention, one with ordinary skill in the art would have found it obvious to modify the device of O'Connor with the thermoelectric cooling device of

Rabin because the cooling device of Rabin is capable of dissipating heat from one area to another (Rabin, 12:20-13:7) as well as converting heat to electrical energy, thus functioning as an additional power generator (Rabin, 13:18-25).

Furthermore, one would have found it obvious to modify the device of O'Connor by adjusting density of the thermoelectric elements according to the temperature profile of the microelectronic die 40 of O'Connor in the manner disclosed by Chu because doing so would allow for lower circuit temperature for a given heat load to be established, provide a more uniform temperature distribution across the electronic device and improve the efficiency of the thermoelectric assembly (Chu, 7:5-13). Specifically, arranging the nano-wires with the higher density proximate to the area of higher temperature (100-110°C), surrounding the area of higher temperature with a lower density of nano-wires proximate to area of intermediate temperature (90-100°C) between the area of higher temperature (100-110 °C) and the remainder of the microelectronic die, surrounding the lower density area with a further lower density proximate to an area of lower temperature (80-90 °C), and an absence of nano-wires at the area of lowest temperature (50-60 °C), which is proximate to the remainder of the microelectronic die.

O'Connor, Rabin and Chu are silent regarding the nano-wires being arranged in concentric ovals as required by current claim. However, it does not appear that the concentric ovals arrangement is critical to the instant application for such concentric ovals arrangement is designed to match the temperature profile of the electronic die (figure 13 of current application); furthermore, Chu already discloses the method of arranging the density of the nano-wires to match the temperature profile of an electronic

die as addressed above. Therefore, the arrangements of the nano-wires are selectable variables of which the selection of shape would be within the technical grasp of an ordinary artesian based on the size, shape and the location of the intended installation/application. Thus, absent contrary support for the criticality of the claimed concentric ovals arrangement, it would have been a matter of obviousness to a person having ordinary skill in the art at the time of the invention to vary/select the shape of the arrangement of the nano-wires in the thermoelectric package of O'Connor, Chu and Rabin (see MPEP 2144.04{IV}{B}).

Addressing claim 25, Rabin discloses a negatively charged trace electrically connected to the first electrode (for cooling function as described in figure 8A, the negatively charged p-type nanowires 222 are connected to the electrode 260) and a positively charged trace to the second electrode (in figure 8A, the n-type nanowires 224 are positively charged, 12:29-13:7).

Response to Arguments

13. Applicant's arguments with respect to claims 6, 8-11 and 21-25 have been considered but are moot in view of the new ground(s) of rejection.

Khan is cited for the disclosure of a temperature distribution profile of a microelectronic die; wherein, the area of highest temperature is concentrically surrounded by areas of successively lower temperature (figure 2B).

With respect to applicant's argument regarding the nano-wires being arranged in an area of higher density, an area of lower density and a further area of lower density that form concentric ovals, the argument is not persuasive in view of the new grounds of rejection as addressed above. It does not appear that the concentric ovals arrangement is critical to the instant application for such concentric ovals arrangement is designed to match the temperature profile of the electronic die (figure 13 of current application); furthermore, Chu already discloses the method of arranging the density of the nano-wires to match the temperature profile of an electronic die as addressed above. Therefore, the arrangements of the nano-wires are selectable variables of which the selection of shape would be within the technical grasp of an ordinary artesian based on the size, shape and the location of the intended installation/application. Thus, absent contrary support for the criticality of the claimed concentric ovals arrangement, it would have been a matter of obviousness to a person having ordinary skill in the art at the time of the invention to vary/select the shape of the arrangement of the nano-wires in the thermoelectric package of the cited references in this office action (see MPEP 2144.04{IV}{B}).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BACH T. DINH whose telephone number is (571)270-5118. The examiner can normally be reached on Monday-Friday EST 7:00 A.M-3:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on (571)272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nam X Nguyen/
Supervisory Patent Examiner, Art Unit 1753

BD
10/21/2009